Self-Referenced 32-kHz Rotating Capacitor Relaxation Oscillator with Chopped Comparator Offset-Voltage Cancellation

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***Abstract*—This work presents a novel relaxation oscillator architecture using a rotating capacitor integrator and a chopped comparator. The oscillator is self-referenced, using the resistor instead of the current source, together with the reference voltage realized with the resistor divider connected to the supply voltage. The oscillator prototype is designed and manufactured in 180 nm technology, typically consumes 1.5 μA at 32 kHz, has a frequency variation of $\pm$0.44% in the temperature range from $-$40 to 105°C and $\pm$0.3% in the power supply range from 1.62 to 1.98 V. The oscillator has a start-up time of 15.4 μs and is operational in the low supply voltage range.**

I. Introduction

The demand for fully integrated, low-power consumption clock generators is growing with the expansion of the mobile and wearable electronic industry. Although the MEMS, XTAL and LC resonators offer significant performance advantages for such applications, they lack cost efficiency due to unacceptable design and assembly complexity, together with excessive die size [1]–[4]. For this reason, relaxation oscillators for systems-on-chip are being studied on a large scale. They have the advantages of compatibility with monolithic integration, low-power consumption, and small device area and are superior to Wien bridge and ring oscillators in terms of frequency stability. Consequently, several advances in relaxation oscillator architectures have been reported in [5]–[10] that achieve good accuracy in temperature and power supply variations while maintaining low-power consumption and area efficient design.

This work extends this research and introduces a novel relaxation oscillator architecture using a self-chopped comparator built on top of the rotating capacitor-integrator block. This improves the performance of the oscillator by canceling the offset-voltage of the comparator. In addition, the current and voltage references that are normally part of clock generation systems are replaced by reference resistor and voltage divider, allowing a more compact device area and further reducing power consumption.

This work is organized as follows. The oscillator architecture is presented in Section II. Section III shows the measurement results together with the performance comparison with other low power frequency relaxation oscillators. The final conclusions are presented in Section IV.

II. Oscillator Architecture

The schematic of the proposed relaxation oscillator with rotating capacitor integrator and chopped comparator is shown in Fig. 1. The oscillator consists of a rotating capacitor block, reference resistor block, reference voltage generator, chopper block, comparator block, and output buffers.

The rotating capacitor block integrates the incoming current from the reference resistor R_{REF}. The polarity rotation of the capacitor at the end of each half-cycle effectively discharges the capacitors, initiating the start of the next half-cycle. With this, only one integrating unit is necessary, effectively reducing the needed on-chip reference capacitance by the factor of two, and significantly improving the duty cycle by eliminating mismatch between the capacitors in two different half-cycles. Furthermore, the output of the integrator block is connected to the chopped comparator, which compares the integration voltage VC with the reference voltage V_{REF} and also provides feedback to the integrator block and chopper control logic, thus maintaining the oscillation. The oscillator assumes non-overlapping signals $B0$ and $XB0$ during the active state, where the non-overlapping generator schematics are omitted in Fig. 1 and its influence on the timing can be neglected because of low frequency of the oscillator.

The detailed operation of the circuit is explained with reference to the waveforms shown in Fig. 2. It is assumed that at $t = t_0$ the voltage reference V_{REF} is set to the value defined by the resistor divider (R_1 and R_2):

$$V_{REF} = V_{DD} \cdot \frac{R_1}{R_1 + R_2}, \tag{1}$$

and all signals are forced by the start circuit to the default state (not shown in the schematics). Consequently, as defined by the state of the signals $B0$ and $XB0$, at $t = t_0$ the circuit is in the state $\Phi 1$, where the rotating capacitor signals $VC1$ and $VC2$ are connected to $VC1 \mapsto GND$ and $VC2 \mapsto VC$, and the comparator input signals $A1$ and $A2$ are mapped as $A1 \mapsto VC$ and $A2 \mapsto V_{REF}$.

Furthermore, the total capacitance connected to the signals $A1 \mapsto VC2 \mapsto VC$ is equal to C_{REF} and it is charged via the reference resistor R_{REF} with the time constant $\tau_{REF} =$

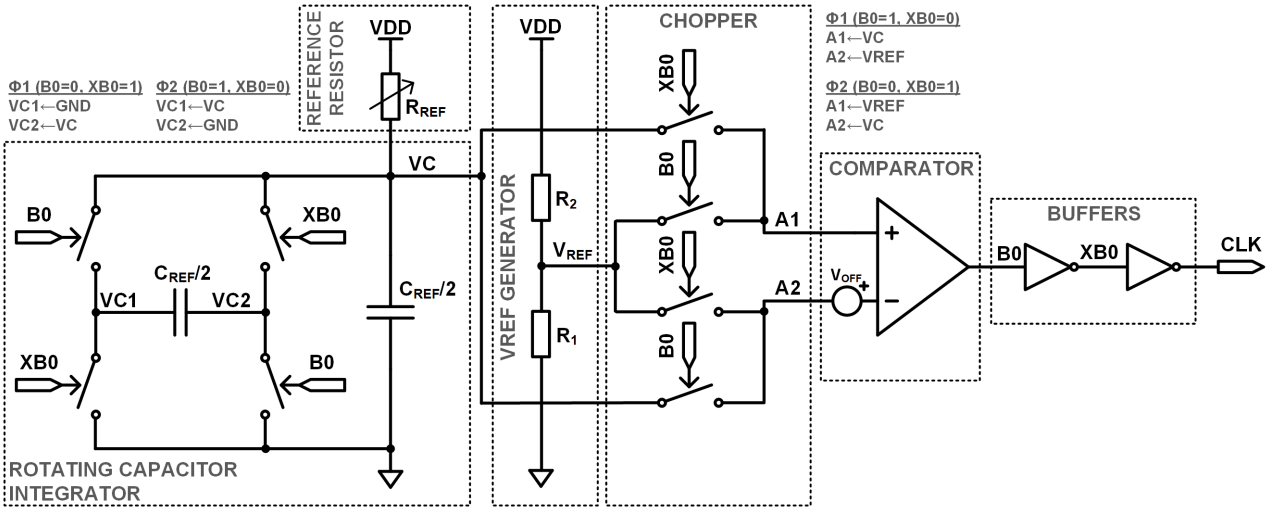

Fig. 1. The simplified schematic of the proposed relaxation oscillator, consisting of a rotating capacitor integrator, reference resistor, voltage reference generator, chopper block, comparator, and buffer block.

$R_{REF} \cdot C_{REF}$. Consequently, the following equation is valid in the time interval $\langle t_0 \rightarrow t_2 \rangle$:

$$A1(t) = VC(t) = V_{DD} \cdot \left[1 - exp\left(-\frac{t - t_0}{\tau_{REF}}\right)\right]. \quad (2)$$

At $t = t_1$ the signal $A1$ becomes equal to the reference voltage $A2 \mapsto V_{REF}$. However, the comparison only starts at $t = t_1'$ when the signal $A1$ becomes equal to $V_{REF} + V_{OFF}$, resulting from the influence of the offset-voltage of the comparator. Furthermore, due to the propagation delay of the comparator, additional time is required to change the state of the comparator output $B0$ from low to high, namely t_{dlh}, meaning the signal $B0$ becomes high at $t = t_2$.

Since the change of the signal $B0$ is followed by the change of the signals $XB0$ and CLK, the state of the chopper and the rotating capacitor changes from Φ_1 to Φ_2 at $t = t_2$. Since the charges of two segments of the capacitor with the capacitance $C_{REF}/2$ at $t = t_{2-}$ are equal, the charges at $t = t_{2+}$ are redistributed between the two capacitors, meaning that $VC1 = VC2 = VC = 0$.

Since the circuit is in state Φ_2, the rotating capacitor signals $VC1$ and $VC2$ are now connected to $VC1 \mapsto VC$ and $VC2 \mapsto GND$, and the comparator input signals $A1$ and $A2$ are mapped as $A1 \mapsto V_{REF}$ and $A2 \mapsto VC$.

Consequently, the total capacitance connected to the signals $A2 \mapsto VC1 \mapsto VC$ is equal to C_{REF} and it is charged via the reference resistor R_{REF} with the time constant $\tau_{REF} = R_{REF} \cdot C_{REF}$. Thus the following applies in the time interval $\langle t_2 \rightarrow t_4 \rangle$:

$$A2(t) = VC(t) = V_{DD} \cdot \left[1 - exp\left(-\frac{t - t_2}{\tau_{REF}}\right)\right]. \quad (3)$$

At $t = t_3$ the signal $A2$ becomes equal to the reference voltage $A1 \mapsto V_{REF}$. However, the comparison had already started at $t = t_3'$ when the signal $A2$ was equal to $V_{REF} - V_{OFF}$, resulting from the influence of the offset-voltage of the comparator. Furthermore, due to the propagation delay of the comparator, additional time is needed to change the state of the comparator output $B0$ from high to low, namely t_{dhl}, which means that the signal $B0$ becomes low at $t = t_4$.

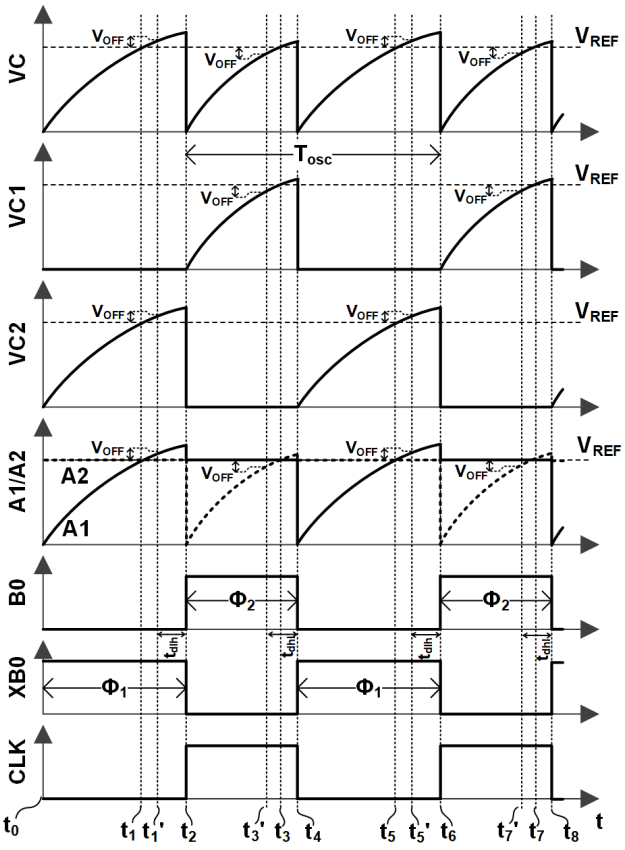

Fig. 2. The signal waveforms of the proposed relaxation oscillator.

Since the change of the signal $B0$ is followed by the change of the signals $XB0$ and CLK, the state of the chopper and the rotating capacitor changes from Φ_2 to Φ_1 at $t = t_4$. Again the charges of two segments of the capacitor are redistributed at $t = t_{4+}$, which means that $VC1 = VC2 = VC = 0$.

Due to identical initial signal conditions and chopper states at the times t_0 and t_4, an oscillation cycle is completely described within this time interval, and the identical operation is then repeated. Therefore the oscillation period can be expressed as the sum of the duration of two half-cycle phases (Φ_1 and Φ_2):

$$T_{osc} = t_{\Phi 1} + t_{\Phi 2}, \tag{4}$$

where

$$t_{\Phi 1} = t_2 - t_0, \tag{5}$$

and

$$t_{\Phi 2} = t_4 - t_2. \tag{6}$$

Taking into account (2)–(6), the duration of the two half-cycle phases can be expressed as follows:

$$t_{\Phi 1} = -\tau_{REF} \cdot ln\left(1 - \frac{V_{REF} + V_{OFF}}{V_{DD}}\right) + t_{dhl}, \tag{7}$$

and

$$t_{\Phi 2} = -\tau_{REF} \cdot ln\left(1 - \frac{V_{REF} - V_{OFF}}{V_{DD}}\right) + t_{dlh}. \tag{8}$$

In addition, by combining (4), (7), and (8), the oscillation period T_{osc} can be expressed as

$$T_{osc} = -\tau_{REF} \cdot ln\left[\left(1 - \frac{V_{REF}}{V_{DD}}\right)^2 - \left(\frac{V_{OFF}}{V_{DD}}\right)^2\right] + t_d, \tag{9}$$

where

$$t_d = t_{dlh} + t_{dlh}. \tag{10}$$

By making the following assumption:

$$\left(1 - \frac{V_{REF}}{V_{DD}}\right)^2 >> \left(\frac{V_{OFF}}{V_{DD}}\right)^2, \tag{11}$$

which is generally valid for this type of oscillators, and also taking into account (1) and (10), the expression for the period of oscillation is reduced to:

$$T_{osc} = 2 \cdot R_{REF} \cdot C_{REF} \cdot ln\left(1 + \frac{R_1}{R_2}\right) + t_d. \tag{12}$$

Considering the operation of the oscillator, choosing larger V_{REF} results in larger signal swing that reduces the influence of noise and propagation delay of the comparator (t_d), however, the assumption made in (11) is not fulfilled if V_{REF} is very close to V_{DD}. If the ratio of the resistors $R1/R2 = e - 1$ is chosen, the reference voltage is set to approximately $V_{REF} = 0.632 \cdot V_{DD}$, fulfilling both conditions. With this, the integrating signal amplitude is appropriate for a comparator with nMOS input pair, and the oscillation period expression simplifies to:

$$T_{osc} = 2 \cdot R_{REF} \cdot C_{REF} + t_d. \tag{13}$$

Seen from the equation, the oscillation period is determined by the time constant defined by the reference capacitor and resistor (R_{REF} and C_{REF}) and the propagation delay of the comparator t_d. Other contributions to the oscillaton frequency that are not considered in the equation are the logic propagation delay, switching non-idealities, the influence of the parasitics, and other process-related effects.

III. Measurement Results

In order to verify the proposed oscillator architecture, the oscillator prototype was designed in 180 nm CMOS technology and 5 test-chip samples were manufactured. The micro-photograph of the chip prototype is shown in Fig. 3. The oscillator consumes 1.5 μA at a nominal power supply of 1.8 V, with an average nominal frequency of 34.5 kHz and a process sensitivity of σ=0.5% before calibrating the center frequency to 32 kHz. The typical measured start-up time is 15.4 μs.

The measured frequency variation versus the temperature and power supply change is shown in Fig. 4 and Fig. 5, respectively. The figures show that the frequency variation versus temperature is $\pm$0.44% in the temperature range from -40 to 105°C, while the frequency variation versus power supply is $\pm$0.3% in the supply range from 1.62 to 1.98 V.

In addition, the frequency of the oscillator was measured in the low supply voltage range, down to 0.9 V. For this test-case the measured frequency error against the supply voltage is shown in Fig. 6, evaluated at different temperatures (-40°C, 25°C, 105°C). From the figure it can be seen that the oscillator frequency is minimally affected at the supply voltage of more than 1.1 V, whereby the relative frequency variation less than $\pm$0.5%.

In the end, the performance comparison between the other recently reported low frequency, energy efficient relaxation oscillators is shown in Table I. First, the proposed oscillator provides a compact design that is smaller or comparable to other 180 nm designs and designs in smaller technology nodes. In addition, although the proposed oscillator is less energy efficient compared to the other designs, it has an excellent frequency stability and a very short start-up time, specifically

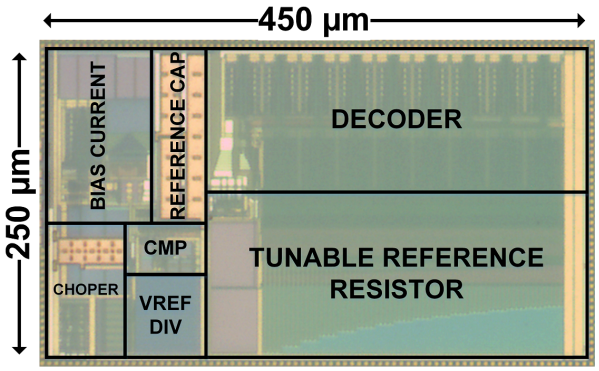

Fig. 3. Die micro-photograph of the manufactured test-chip. The overall area of the oscillator is 0.113 mm^2.

TABLE I
PERFORMANCE COMPARISON OF RECENTLY REPORTED LOW-POWER ON-CHIP RELAXATION OSCILLATORS

	Year	Process [nm]	Area [mm^2]	Freq. [kHz]	Power [μW]	Supply [V]	Temperature variation [%]	Line sensitivity [%]	Energy/cycle [nW/kHz]	Start-up time
Paidimarri [6]	2016	65	0.032	18.5	0.13	1	±0.55 @−40∼90°C	±0.25 @0.95∼1.05V	7.03	4 cyc.
Sebastiano [7]	2009	65	0.11	100	41	1.2	±1.1[a] @−22∼85°C	±0.1 @1.12∼1.39V	410	10 ms
Tsubaki [8]	2013	180	0.105	32.5	0.472	1	±0.84 @−40∼100°C	±0.44 @1.0∼1.8V	14.5	108 μs
Tokairin [9]	2012	90	0.12	100	0.28	0.8	±0.68 @−40∼90°C	±0.82 @0.725∼0.9V	2.80	1 cycle
Asano [10]	2016	180	0.19	32.7	0.054	0.85	±1.19 @−40∼80°C	±0.89 @0.85∼1.85V	1.66	NA
This work	**2021**	**180**	**0.113**	**32**	**2.7**	**1.8**	**±0.44 @−40∼105°C**	**±0.3 @1.62∼1.98V**	**84**	**15.4 μs**

[a] External references.

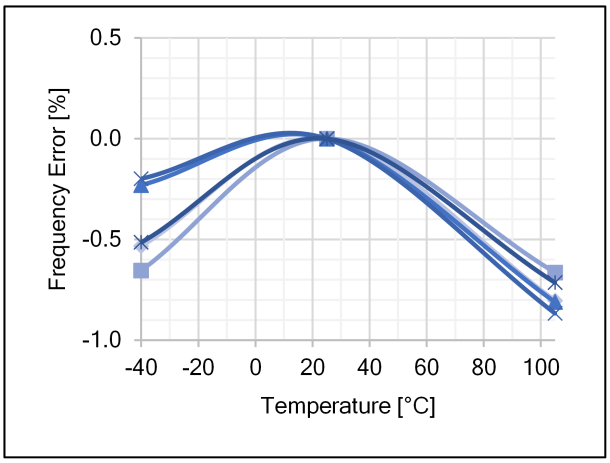

Fig. 4. Frequency error vs. temperature, measured in the temperature range from −40 to 105°C on 5 test-chip samples.

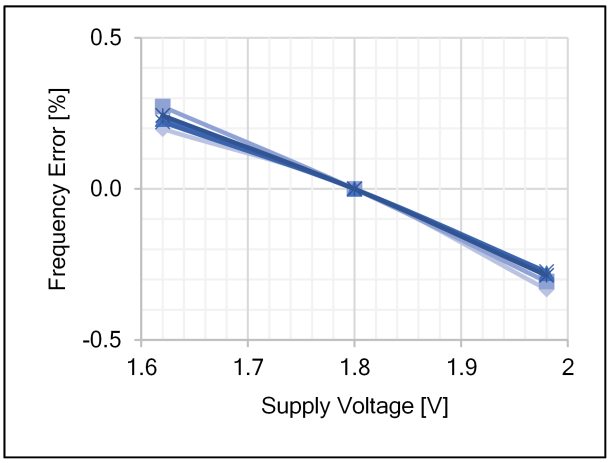

Fig. 5. Frequency error vs. power supply voltage, measured in the power supply range from 1.62 to 1.98 V on 5 test-chip samples.

less than half of the period. Finally, it is worth mentioning that reducing the power level of the designed oscillator is feasible at the price of lower frequency accuracy.

IV. CONCLUSION

In this work a self-referenced low power relaxation oscillator was presented. After implementing the offset voltage compensation with a chopped comparator on the variable capacitor integrator, the oscillator shows a frequency deviation of ±0.44% in the temperature range from −40 to 105°C and ±0.3% in the power supply range from 1.62 to 1.98 V.

The proposed architecture is fully compatible with monolithic integration, has relatively low-power consumption, short start-up time, and a wide operating power supply range, and is also suitable for various portable, battery-powered and mobile applications.

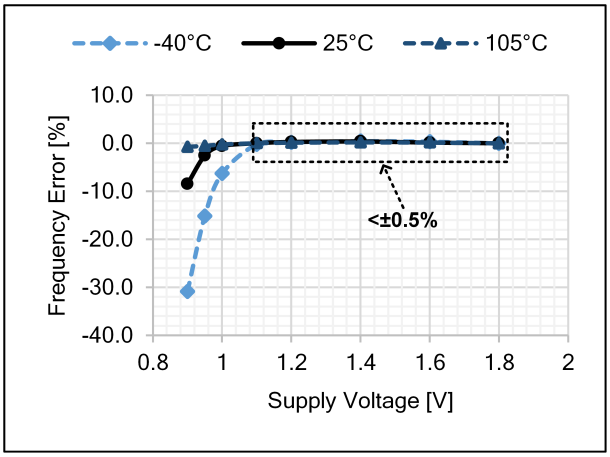

Fig. 6. Frequency error vs. power supply voltage, measured in the power supply range from 0.9 to 1.8 V at three temperatures (−40°C, 25°C, 105°C) on one test-chip sample.

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